TITLE OF THE INVENTION

Adiabatic Charging Register Circuit

ABSTRACT OF THE DISCLOSURE

An adiabatic charging register circuit comprising a plurality of n-channel MOSFET's and a plurality of p-channel MOSFET's, is operated by a clock signal which has a gradually rising and a gradually falling waveform generated by using a charge recycle power source in which charge supplied to a load is at least partially collected to said charge recycle power source, and following inequality is satisfied;

$$|V_{TN}| + |V_{TP}| \geq VDD$$

where V_{TN} is threshold of an n-channel MOSFET, V_{TP} is threshold of a p-channel MOSFET, and VDD is output voltage of said charge recycle power source.

(Fig.4)